HBS-Compatible Driver and Receiver Monolithic IC XL1191

Features

- Built in dynamic impedance matching function
- Built in decoding error correction function
- Built in decoding signal correction function
- Built in hardware codec
- Enhanced anti-interference ability
- Support multiple network topologies
- Support adjusting load balancing time
- Simple circuit design
- High reliability
- Communication speed adaptation from 9.6kbps to 57.6kbps
- Operating temperature -40℃~125℃
- Available in QFN3*3-16 package

Applications

- Central Air Conditioner
- HVAC
- Smart Home
- Remote Monitoring and Sensing

General Description

The XL1191 conforms to the HBS(Home Bus) specification, built in dynamic impedance matching function, decoding error correction function, decoding signal correction function, adjusting load balancing time, and has functions for the reception and transmission of data. AMI is adopted for the waveforms of signals handled by the transmission and reception units, designed for connection to twisted-pair lines. The IC can be driven by a single 5V power supply, and incorporates an output transistor to reduce the number of external components required.

XL1191 is a special hardware encoding and decoding chip for DC carrier communication. It supports DC carrier and nonpolar connection. It has flexible bus topology and strong anti-interference ability. It can communicate while powered by teisted pair cablies. The communication distance can reach 1000m. It has built-in protection module, simple peripheral circuit and high reliability.

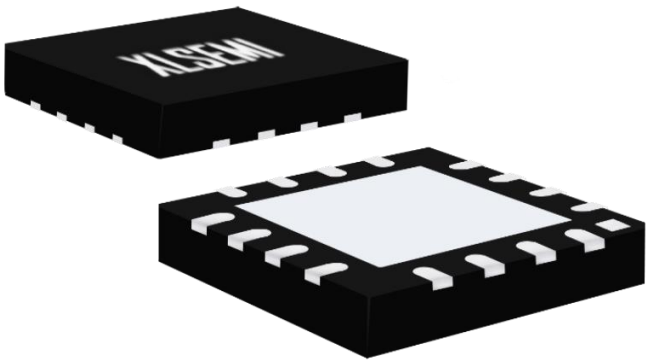


Figure1. Package Type of XL1191

Pin Configurations

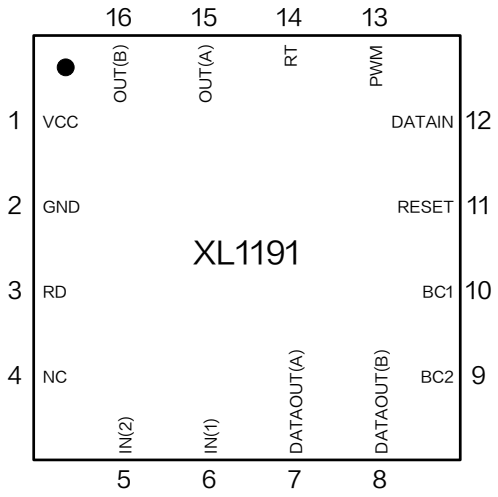


Figure2. Pin Configuration of XL1191 (Top View)

Table 1 Pin Description

Pin Number	Pin Name	Description
1	VCC	Supply voltage input pin.
2	GND	Ground pin (The Exposed PAD is GND).
3	RD	Signal correction pin. Connect to GND through a resistor and adjust the duty cycle of DATA OUT (B).
4	NC	No connected.
5	IN(2)	Bus signal receiving pin 2.
6	IN(1)	Bus signal receiving pin 1.
7	DATA OUT(A)	Data output pin A.
8	DATA OUT(B)	Data output pin B.
9	BC2	Boost capacitor pin 2.
10	BC1	Boost capacitor pin 1.
11	RESET	Reset control pin.
12	DATA IN	Data input pin.
13	PWM	PWM signal pin.
14	RT	Dynamic load balancing time adjustment pin. Connect an external resistor to the GND pin and connect it to the VCC pin when not in use.
15	OUT(A)	Bus signal transmission pin A.
16	OUT(B)	Bus signal transmission pin B.

Function Block

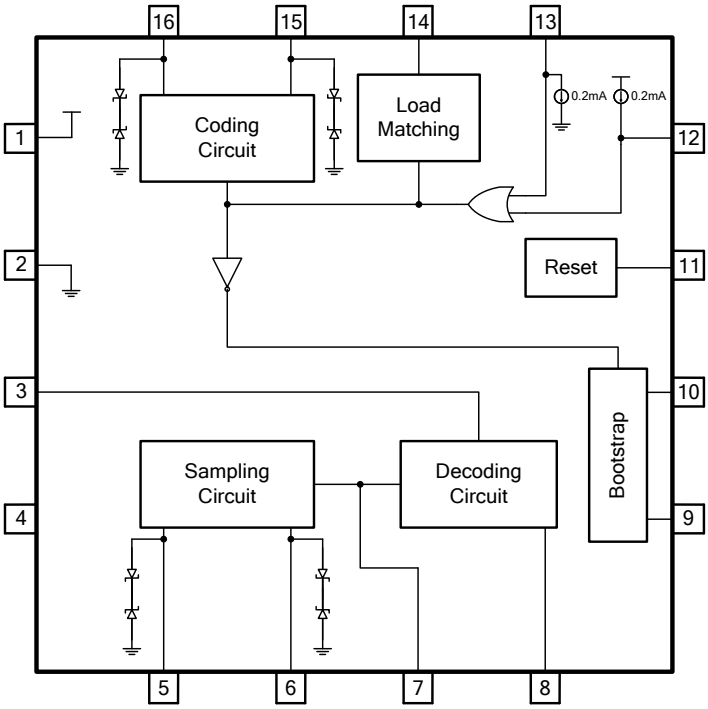


Figure3. Function Block Diagram of XL1191

Typical Application Circuit

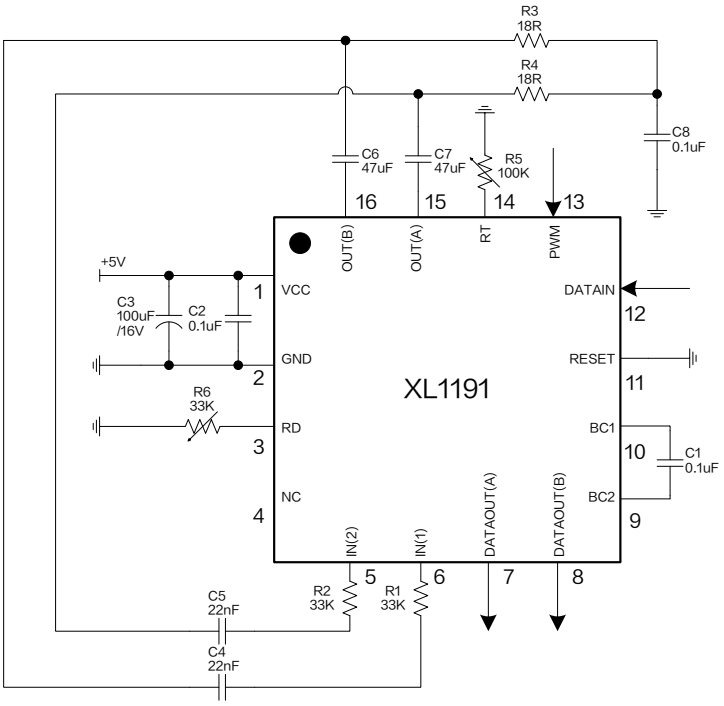


Figure4. XL1191 Typical Application Circuit

Ordering Information

Order Information	Marking ID	Package Type	Eco plan	Packing Type Supplied As
XL1191	XL1191	QFN3*3-16	RoHS & HF	5000 Units on Tape & Reel

Absolute Maximum Ratings (T_A=25℃)

Parameter	Symbol	Value	Unit
Operating power supply voltage (VCC)	V_{CCOP1}	4.5 ~ 5.5	V
Recommended power supply voltage range	V_{CCOP2}	4.75 ~ 5.25	V
Power supply voltage (VCC)	V_{CC}max.	−0.3 ~ 7	V
Pin9 voltage	V_{PIN3}	−0.3 ~ 10	V
Other pins voltage	V	−0.3 ~ VCC	V
Power Dissipation	P_D	450	mW
Operating Junction Temperature	T_J	−40 ~ 125	℃
Storage Temperature	T_{STG}	−40 ~ 125	℃
Lead Temperature (Soldering, 10 sec)	T_{LEAD}	260	℃
ESD (HBM)(PIN15,PIN16)		>8000	V
ESD (HBM)(Other PINs)		>3000	V

Note1: Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note2: Pins 5,6,15 and 16 have built-in bus burr voltage absorption circuit. They can absorb positive and negative burr voltage, and the clamping voltage is designed to be positive and negative 7.2V.

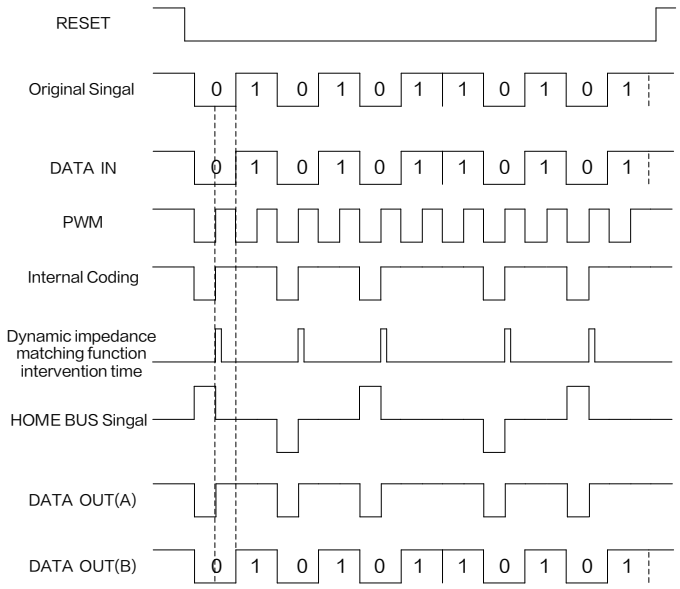
XL1191 Electrical Characteristics

VCC=5V, GND=0V, T_A=25℃; F_{PIN12}=9.6KHz(Duty=50%), F_{PIN13}=19.2KHz(Duty=50%), PIN11=0V, R5=100KΩ, R6=33KΩ, R_L=36Ω, System parameters test circuit figure4, unless otherwise specified.

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current 1	ICCO	PIN11=5V		10		mA
Power supply current 2	ICCON1	PIN13=0V		68		mA
Power supply current 3	ICCON2			40		mA
Transmission output voltage	V_{TO}	Both pins 15 and 16	3.8	4.2	4.6	V_{P-P}
Transmission waveform symmetry	V_{TR}	$V_{TO}1/V_{TO}2$	0.75	1.0	1.25	
Reception Sensitivity	V_{RS}			0.75		V_{P-P}
Noise resistance	V_{RN}	Level at which no errors are output	0.55			V_{P-P}
Input impedance	R_{IN}	Both pins 5 and 6	25	36	46	KΩ
Transmission delay time 1	T_d1	cf. transmit/receive waveform diagrams		0.6		uS
Transmission delay time 2	T_d2	cf. transmit/receive waveform diagrams		2.7		uS
Transmission delay time 3	T_d3	cf. transmit/receive waveform diagrams		3.3		uS
Reception output H voltage	V_{ROH}		4.5			V
Reception output L voltage	V_{ROL}				0.5	V
H level input voltage 1	V_{LIH}	PIN12	2.4			V
L level input voltage 1	V_{LIL}	PIN12			0.6	V
H level input current 1	I_{LIH}	V_{DATAIN}=2.4V			10	uA
L level input current 1	I_{LIL}	V_{DATAIN}=0.4V			−400	uA
H level input voltage 2	V_{LIH}	PIN13	2.4			V
L level input voltage 2	V_{LIL}	PIN13			0.6	V
H level input current 2	I_{LIH}	V_{PWM}=2.4V			400	uA
L level input current 2	I_{LIL}	V_{PWM}=0.4V			400	uA
Bootstrap output H voltage	V_{BR}		7.5	8.0		V

Timing Chart

Data Transceiver Timing Chart



Transmission delay time

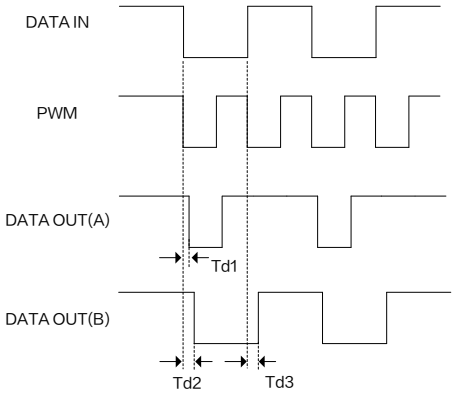


Figure5. XL1191 Timing diagram

Note 1: The peripheral components in the block diagram are the constants for Data Rates 9.6kbps. If the data rates is low, larger values should be chosen for the coupling capacitors between the receive and transmit pins and the bus line and for the capacitor connecting pins 9 and 10.

Note 2: The Pin13 of the chip can access the Data Rates 19.2kbps square wave signal, Realize Pin12 signal (Data Rates 9.6kbps) and Pin13 signal synchronization (the Pin12 data signal is synchronized at the falling edge of the Pin13 square wave signal) to ensure that the hardware coding is correct.

Note 3: Pin7 of the chip outputs the demodulated 19.2kbps signal, and Pin8 outputs the decoded 9.6kbps signal (equivalent to doubling the low-level time of Pin7 output signal).

Note 4: The current limit function is built into this IC. There is a possibility that IC generates heat when the output terminal is short. However, the characteristic changes depending on the substrate condition. Please evaluate IC in the set.

Note 5: The ceramic capacitor should be placed closer the VCC and GND pins to eliminate noise. Increase the grounding vias to decrease the Parasitic parameter.

Function Description

Dynamic impedance matching function

XL1191 has a built-in dynamic impedance matching function to improve the bus signal. When the rising edge of the internal coding signal is detected, the built-in matching resistors are briefly connected in parallel to PIN15 and PIN16, and PIN14 is connected to GND through a resistor to adjust the dynamic impedance matching time. This function can be turned off by connecting PIN14 to VCC.

Decoding signal correction function

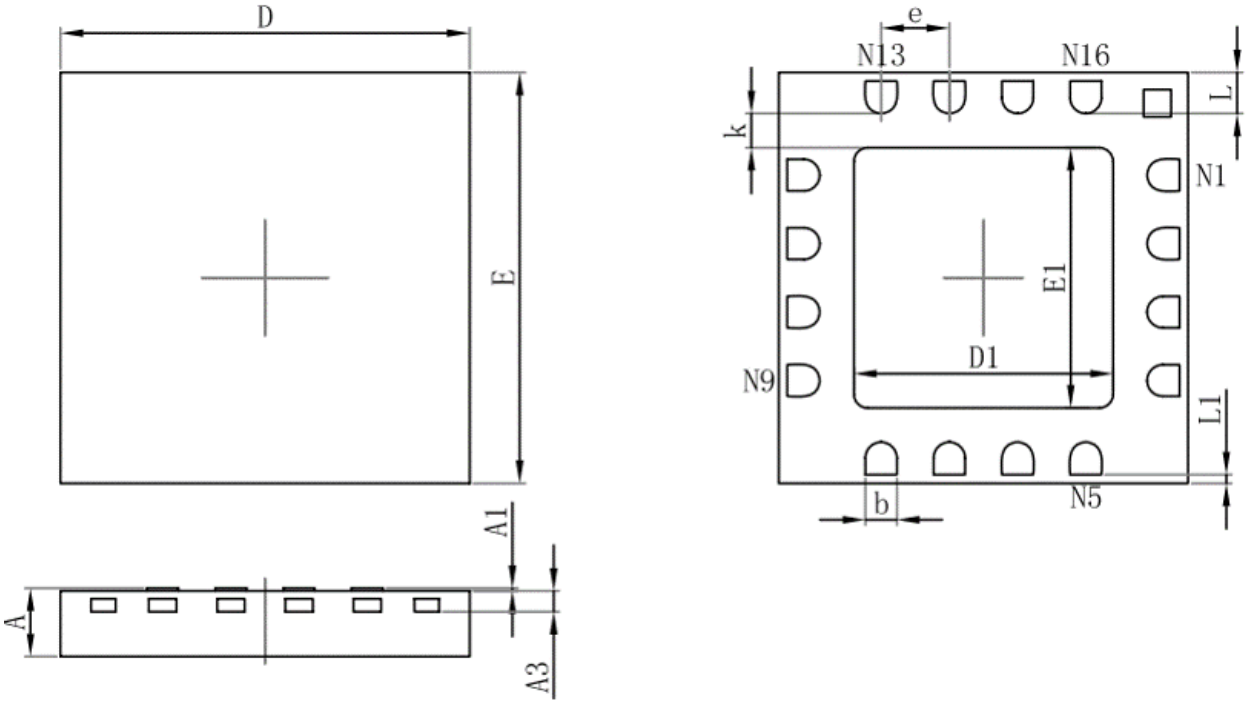
XL1191 has a decoding signal correction function. In the case of long-distance communication, the bus parasitic parameter is large, and the signal transmitted on the bus is affected by the bus parasitic parameter and will turn to a slower level in the middle of the level, resulting in insufficient high level pulse width of the chip's decoding signal, which affects the quality of communication. PIN3 is connected to GND through a resistor, and the resistor value can be adjusted to compensate for the high level pulse width of the PIN8.

Decoding error correction function

XL1191 has built-in decoding and error correction function. It can solve errors caused by bus interference or oscillation, improve decoding accuracy and stability.

Package Information

QFN3*3-16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.152 REF.		0.006 REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	1.800	2.000	0.071	0.079
E1	1.800	2.000	0.071	0.079
k	0.200	–	0.008	–
b	0.230	0.330	0.009	0.013
e	0.500 REF.		0.020 REF.	
L	0.250	0.350	0.010	0.014
L1	0.013	0.113	0.001	0.004

Important Notice

XLSEMI reserve the right to make modifications, enhancements, improvements, corrections or other changes without notice at any time. XLSEMI does not assume any liability arising out of the application or use of any product described herein; neither does it convey any license under its patent rights, nor the rights of others. XLSEMI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using XLSEMI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards. XLSEMI warrants performance of its products to the specifications applicable at the time of sale, in accordance with the warranty in XLSEMI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent XLSEMI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

For the latest product information, go to www.xlsemi.com.